
معماری کامپیوتر

جلسه دوم: یادآوری مباحث از مدار منطقی

ادامه فصل یک و قسمتی از فصل دو

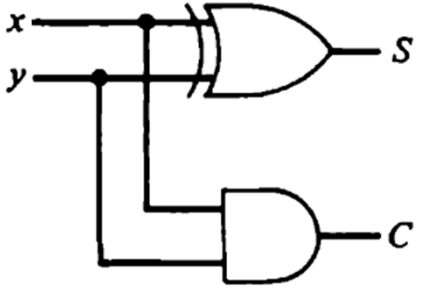
جمع کننده تا دیکدر

- جمع کننده
- فلیپ فلاپ SR
- فلیپ فلاپ D
- فلیپ فلاپ JK و T
- فلیپ فلاپ حساس به سطح و لبه
- جداول تحریک فلیپ فلاپ ها
- مدار ترتیبی
- لیست تمرینات فصل یک
- دیکدر
- توسعه دیکدر ها

نیم جمع کننده

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(a) Truth table



(b) Logic diagram

Figure 1-16 Half-adder.

$$S = x'y + xy' = x \oplus y$$

$$C = xy$$

تمام جمع کننده

TABLE 1-2 Truth Table for Full-Adder

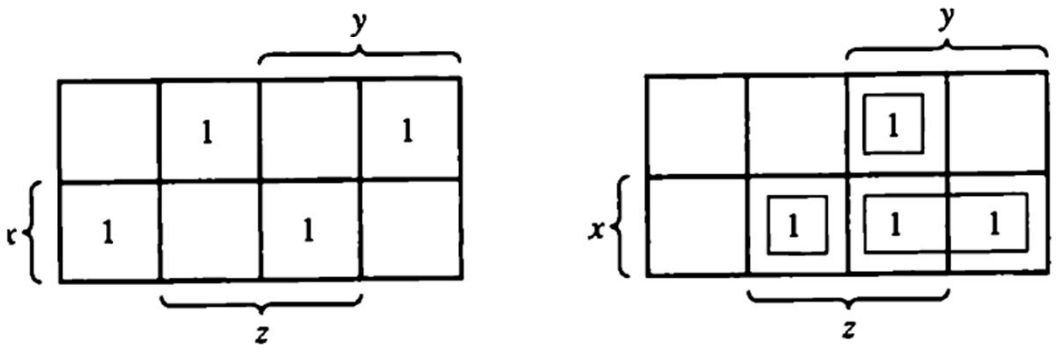
Inputs			Outputs	
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$C = xy + (x'y + xy')z$$

$$S = x \oplus y \oplus z$$

$$C = xy + (x \oplus y)z$$

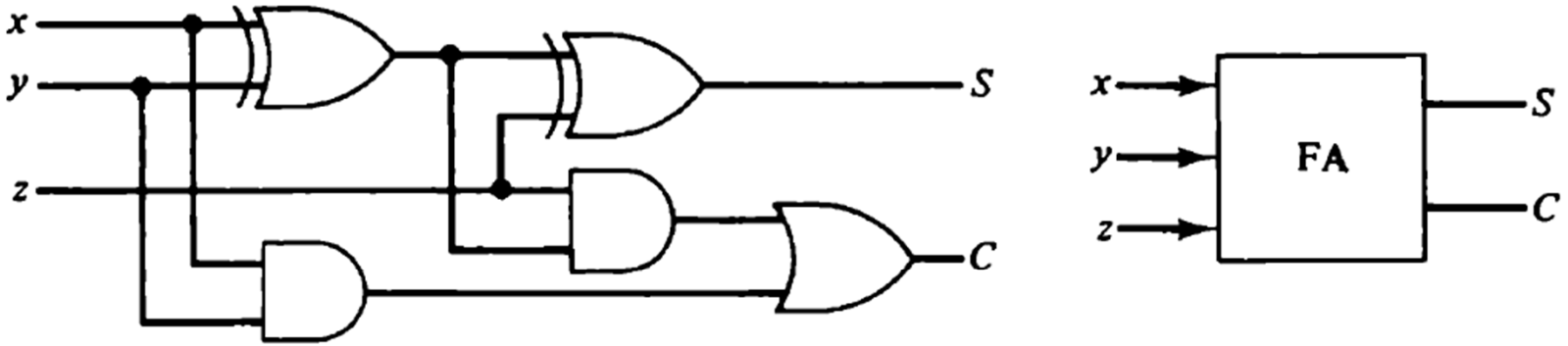
Figure 1-17 Maps for full-adder.



$S = x'y'z + x'yz' + xy'z' + xyz$

$C = xy + xz + yz$

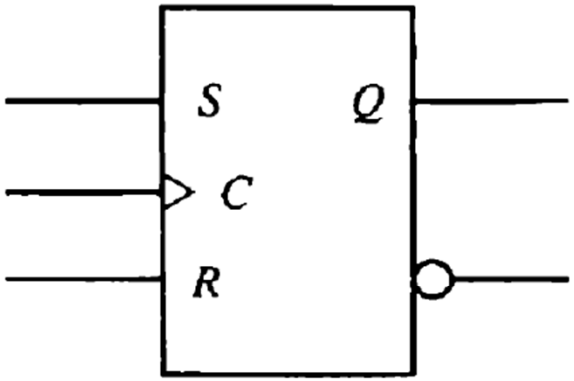
تمام جمع کننده



(a) Logic diagram (b) Block diagram

Figure 1-18 Full-adder circuit.

فلیپ فلاپ SR



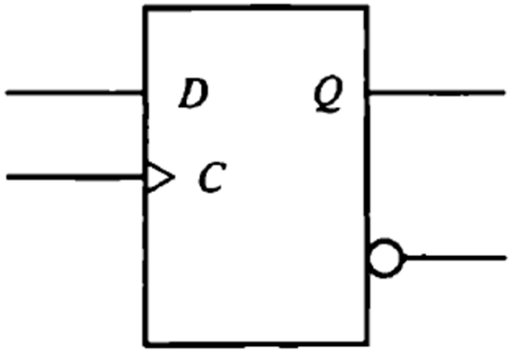
(a) Graphic symbol

S	R	Q (t + 1)	
0	0	Q (t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	?	Indeterminate

(b) Characteristic table

Figure 1-19 SR flip-flop.

فليپ فلاپ D



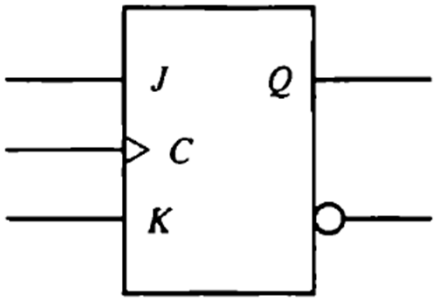
(a) Graphic symbol

D	Q (t + 1)	
0	0	Clear to 0
1	1	Set to 1

(b) Characteristic table

Figure 1-20 *D* flip-flop.

فلیپ فلاپ JK و T

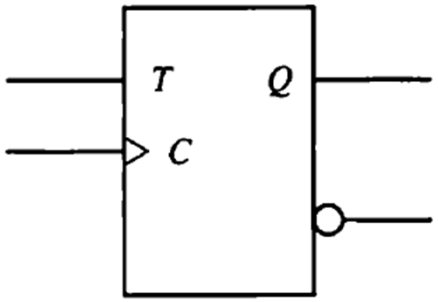


(a) Graphic symbol

J	K	Q (t + 1)	
0	0	Q (t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q′ (t)	Complement

(b) Characteristic table

Figure 1-21 *JK* flip-flop.

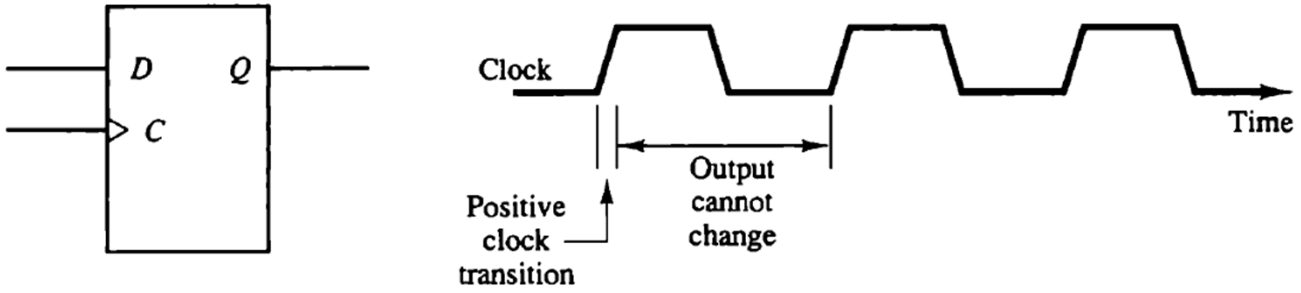


(a) Graphic symbol

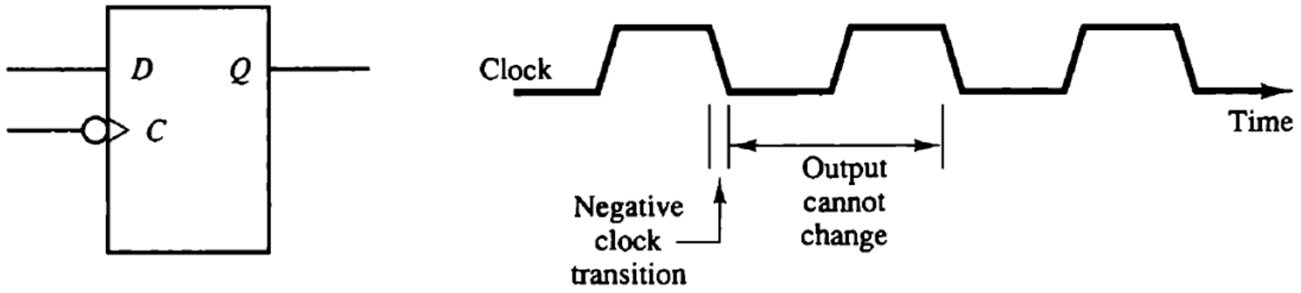
T	Q (t + 1)	
0	Q (t)	No change
1	Q′ (t)	Complement

(b) Characteristic table

فلیپ فلاپ حساس به سطح و لبه



(a) Positive-edge-triggered *D* flip-flop.



(b) Negative-edge-triggered *D* flip-flop.

جداول تحریک فلیپ فلاپ ها

TABLE 1-3 Excitation Table for Four Flip-Flops

SR flip-flop

$Q(t)$	$Q(t+1)$	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

D flip-flop

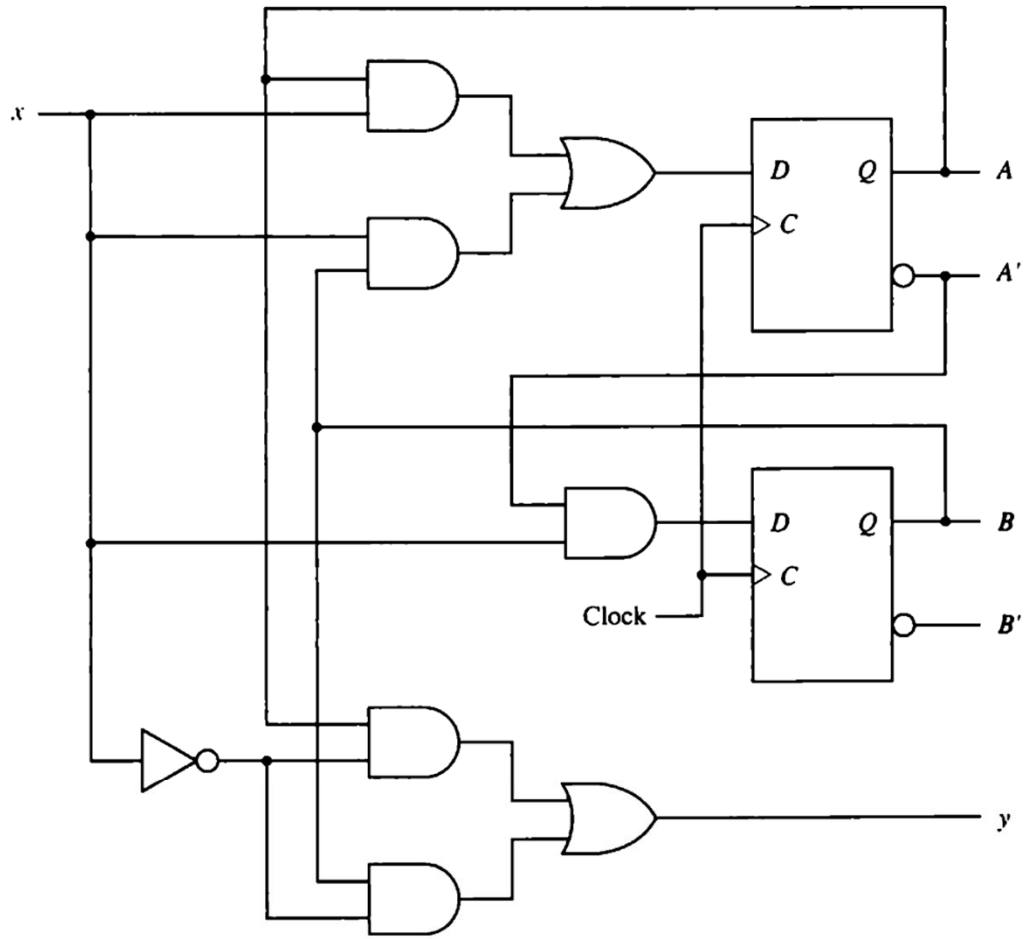
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

T flip-flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

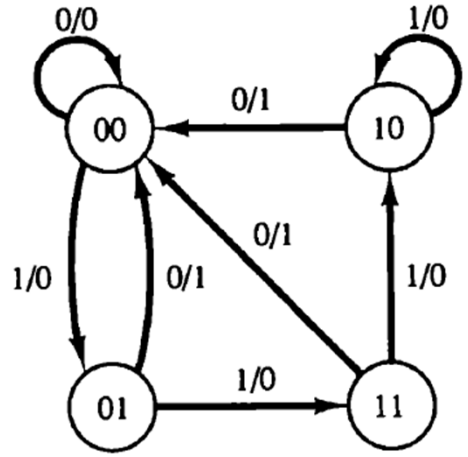

x
D
Q
C
A
A'
D
Q
C
B
B'
Clock
y

$$D_A = Ax + Bx$$

$$D_B = A'x$$

$$y = Ax' + Bx'$$

$$D_A = Ax + Bx \qquad D_B = A'x$$



$$y = Ax' + Bx'$$

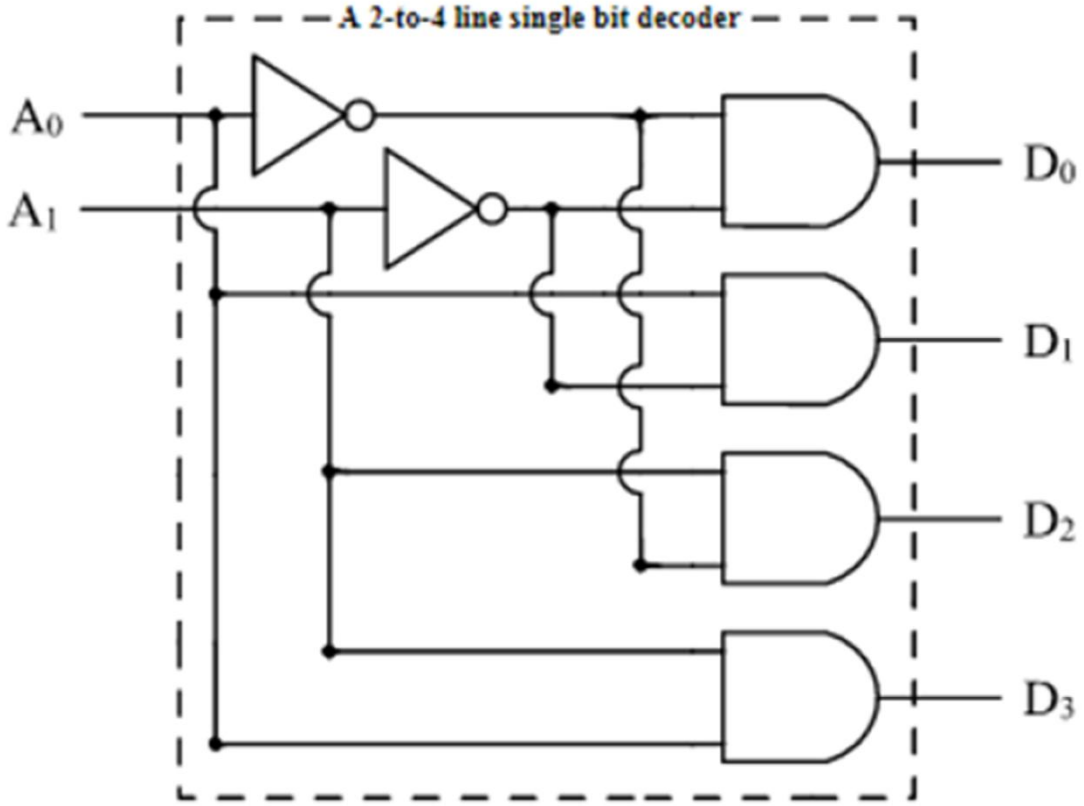
TABLE 1-4 State Table for Circuit of Fig. 1-25

Present state		Input	Next state		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

لیست تمرین های مهم فصل یک

- ۲
- ۳
- ۴
- ۸
- ۹
- ۱۰
- ۱۷
- ۱۹

دیکدر



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

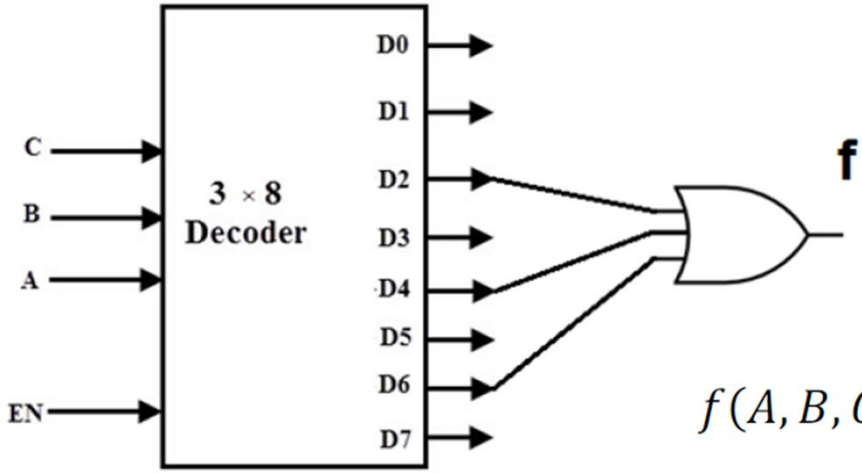
$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

$$D_3 = A_1 \cdot A_0$$

پیاده سازی تابع با دیکدر



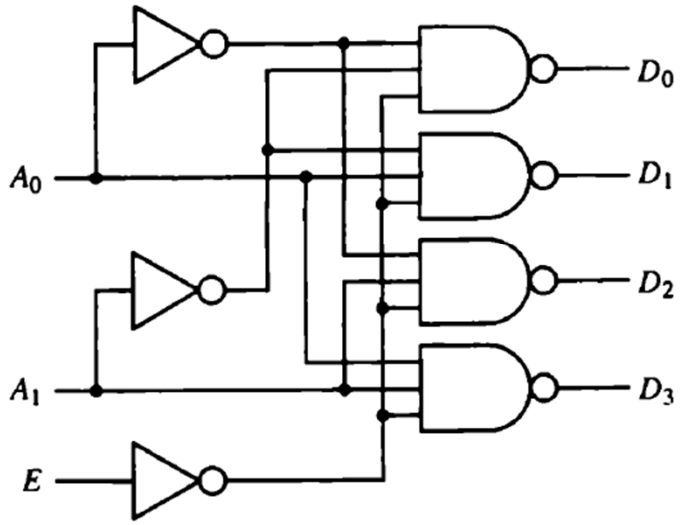
$$f(A,B,C) = \sum m(2,4,6)$$

TABLE 2-1 Truth Table for 3-to-8-Line Decoder

Enable	Inputs			Outputs							
E	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	×	×	×	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

دیکدر NADN

Figure 2-2 2-to-4-line decoder with NAND gates.



(a) Logic diagram

E	A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	×	×	1	1	1	1

(b) Truth table

توسعه دیکدر ها

Figure 2-3 A 3 × 8 decoder constructed with two 2 × 4 decoders.