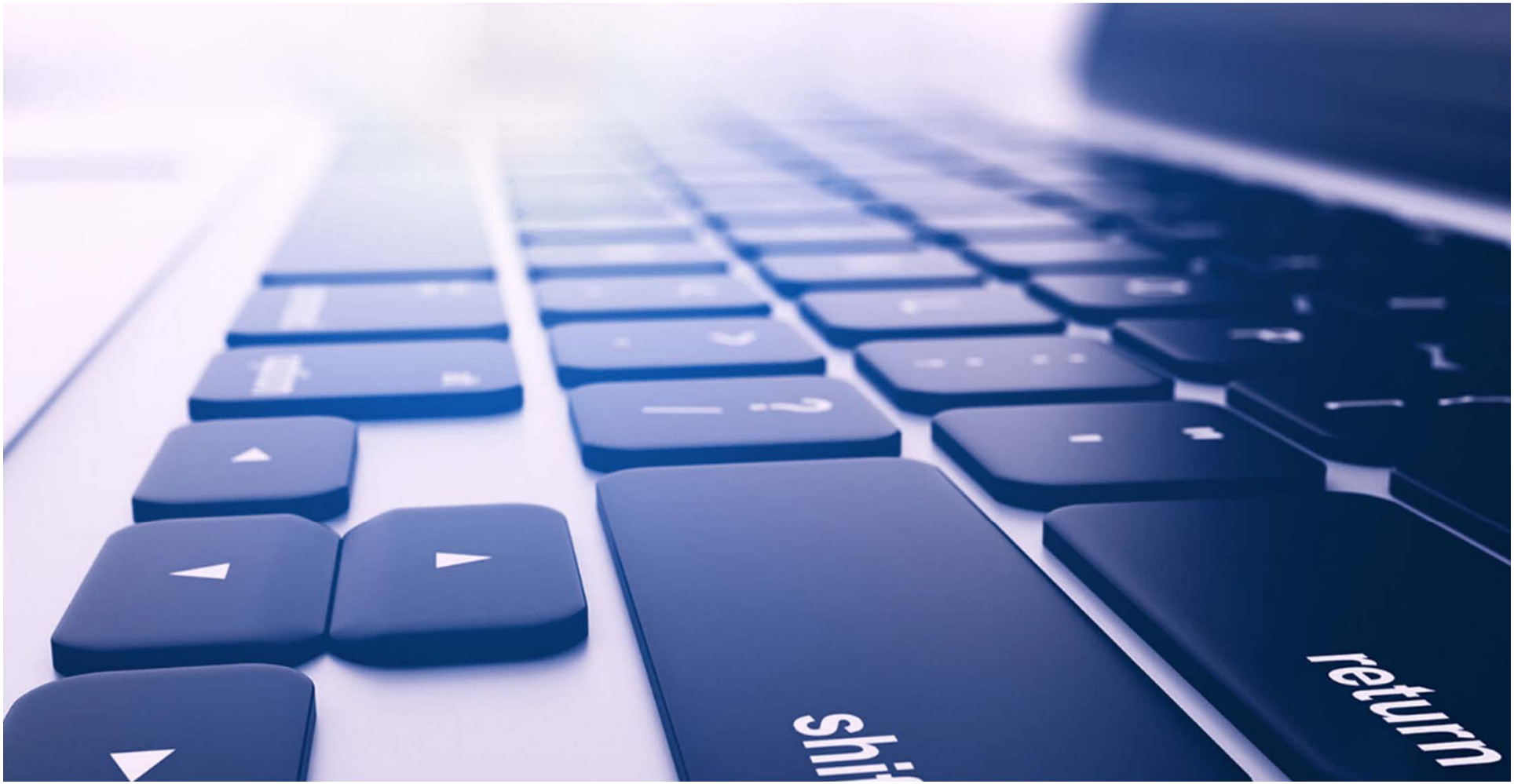

معماری کامپیوتر

جلسه سوم: یادآوری مباحث از مدار منطقی
از مالتی پلکسر تا انتهای فصل دو



- مالتی پلکسر
- پیاده سازی با مالتی پلکسر
- رجیستر
- شمارنده
- واحد حافظه
- تمرینات مهم فصل دو

مالتی پلکسر

Figure 2-4 4-to-1-line multiplexer.

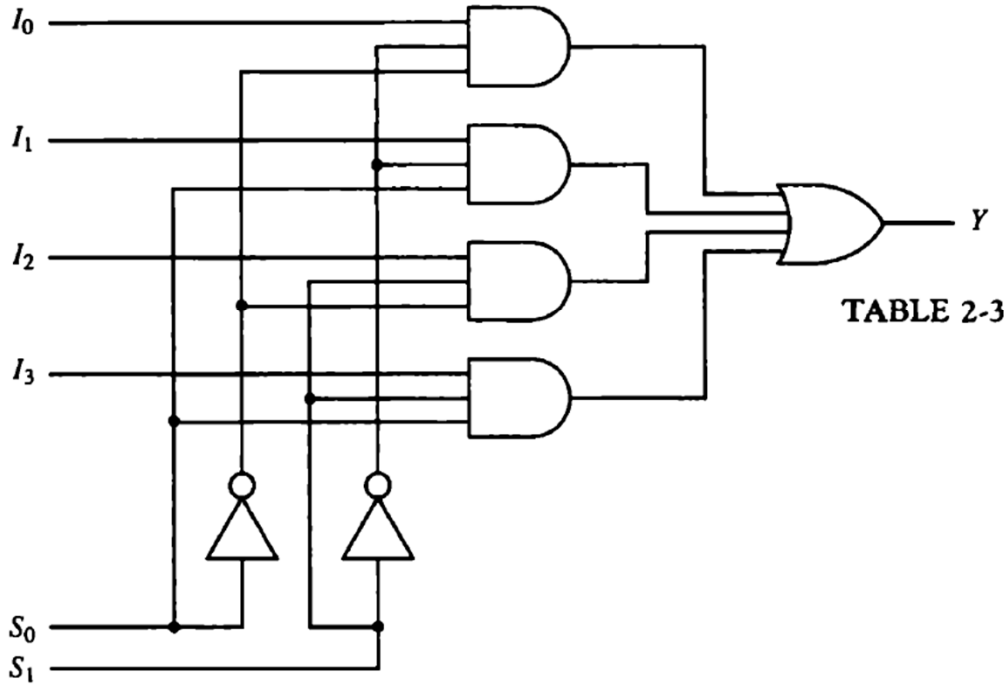


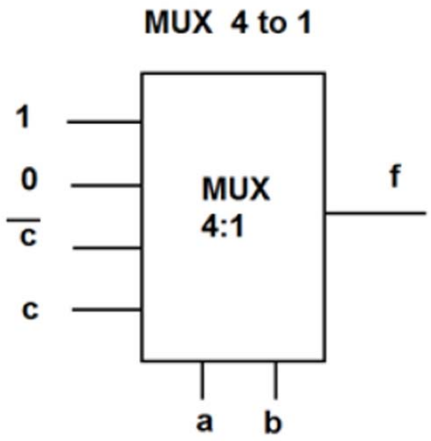
TABLE 2-3 Function Table for 4-to-1-Line Multiplexer

Select		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

پیاده سازی توابع با مالتی پلکسر

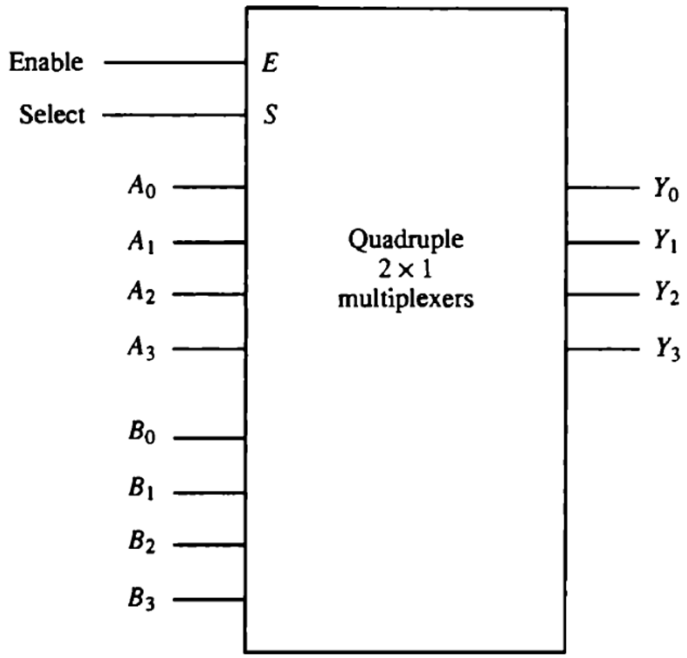
مثال تابع $f(a,b,c) = \sum m(0,1,4,7)$

را با یک مالتی‌پلکسر ۴:۱ پیاده‌سازی کنید.



a	b	c	f	
0	0	0	1	1
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	$\overline{c}$
1	0	1	0	
1	1	0	0	c
1	1	1	1	

مالتی پلکسر چهار کاناله



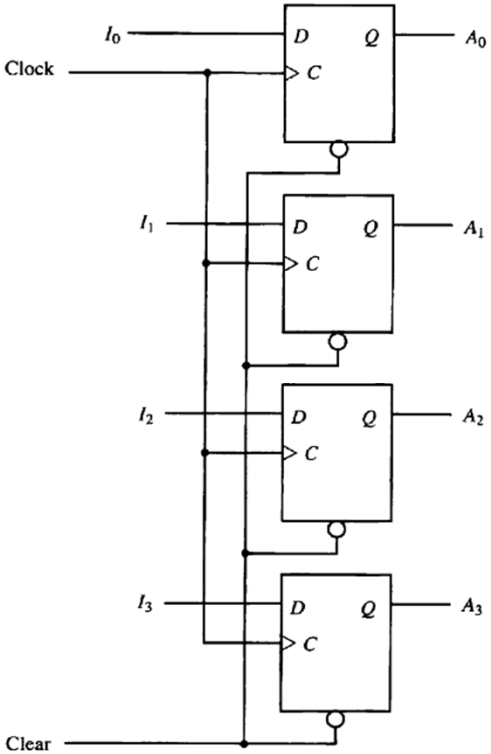
(a) Block diagram

E	S	Y
0	×	All 0's
1	0	A
1	1	B

(b) Function table

Figure 2-5 Quadruple 2-to-1 line multiplexers.

رجیستر ها (ثبات ها)



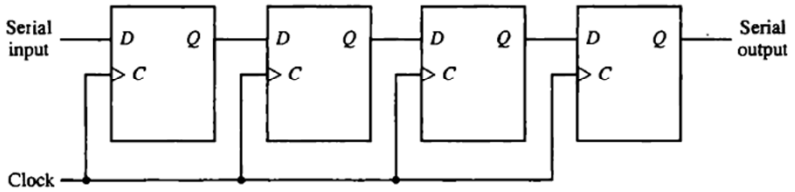


Figure 2-8 4-bit shift register.

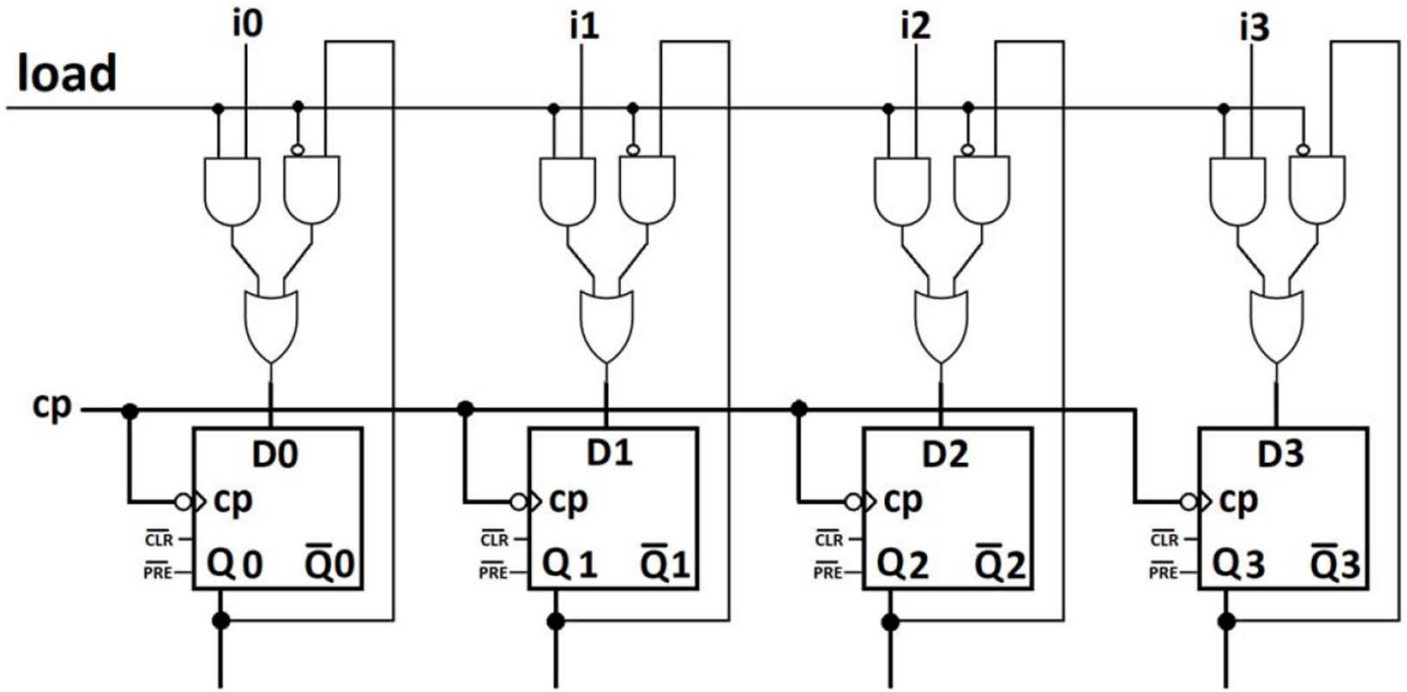

load
i0
i1
i2
i3
cp
D0
D1
D2
D3
cp
CLR
PRE
Q 0
Q0
Q 1
Q1
Q2
Q2
Q3
Q3

TABLE 2-4 Function Table for Register of Fig. 2-9

Mode control		
S_1	S_0	Register operation
0	0	No change
0	1	Shift right (down)
1	0	Shift left (up)
1	1	Parallel load

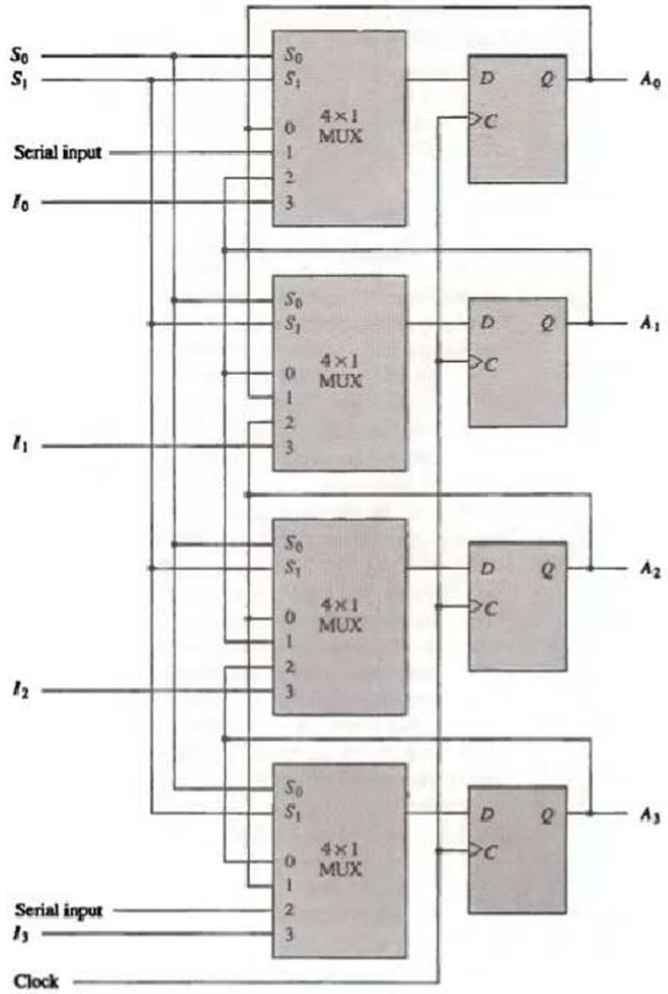
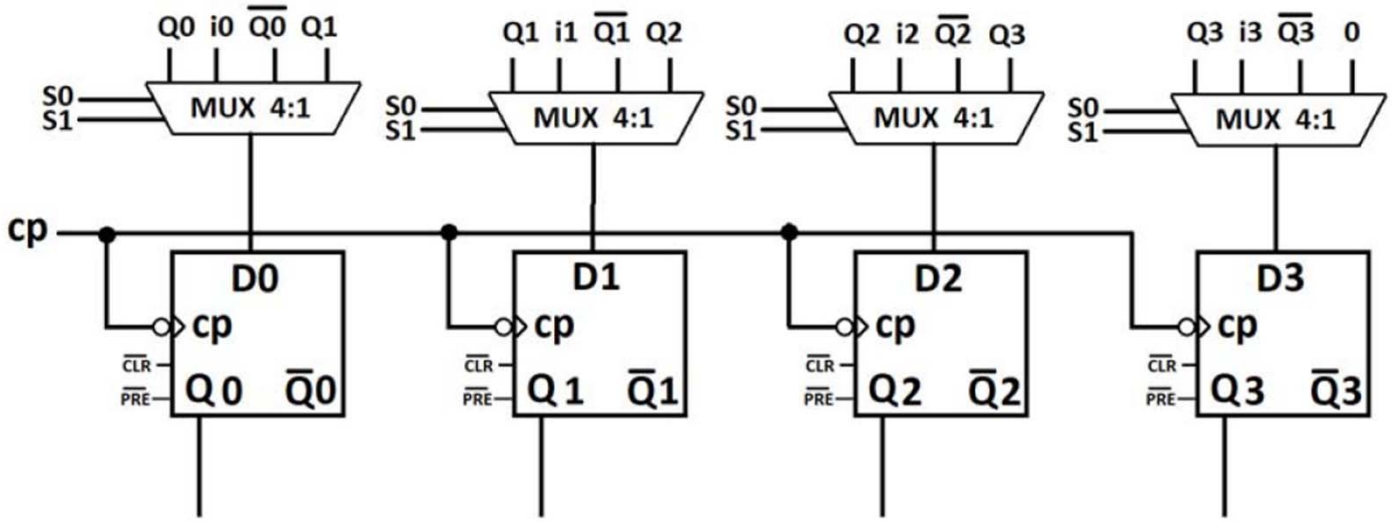
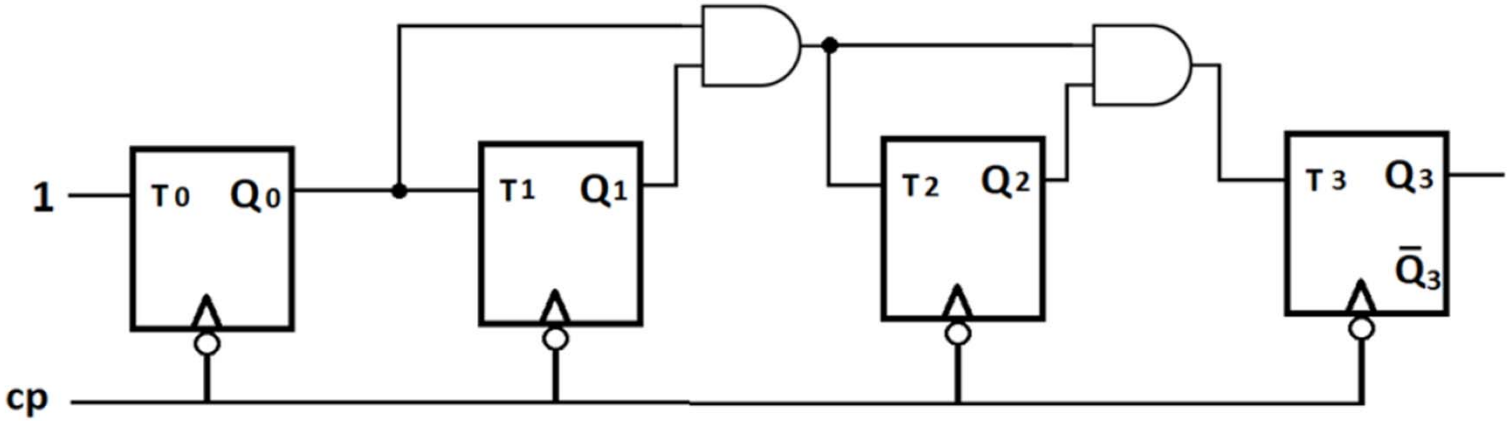


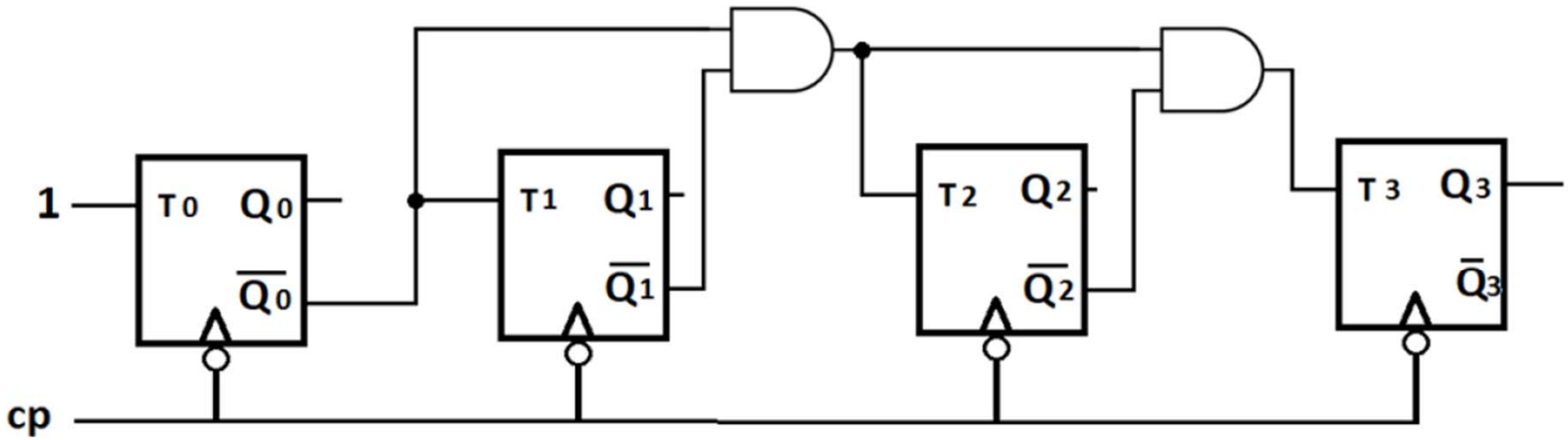
Figure 2-9 Bidirectional shift register with parallel load.



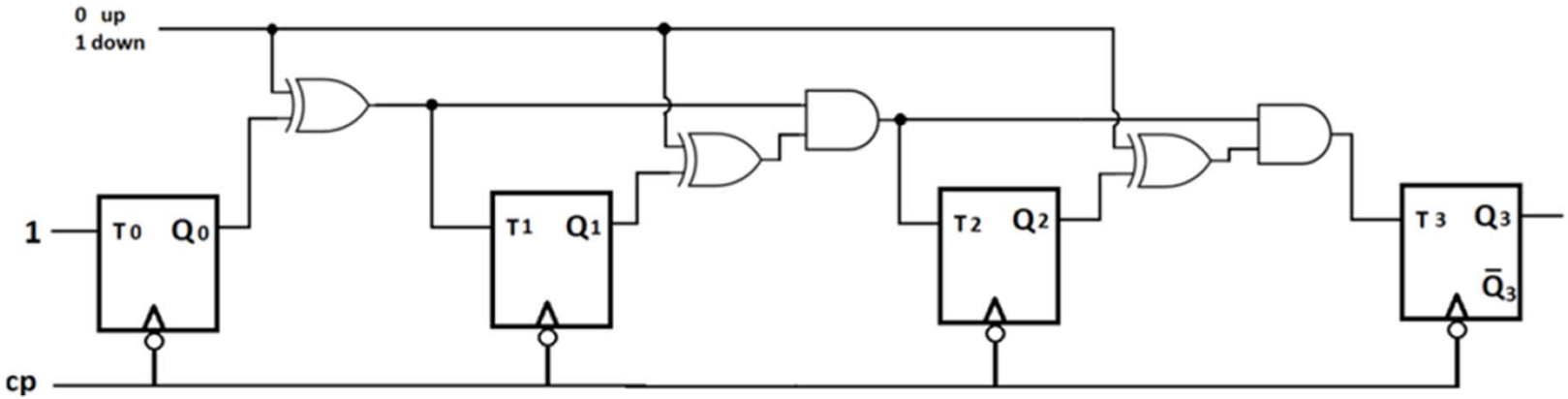
S1	S0	function
0	0	hold
0	1	load
1	0	toggle
1	1	left shift

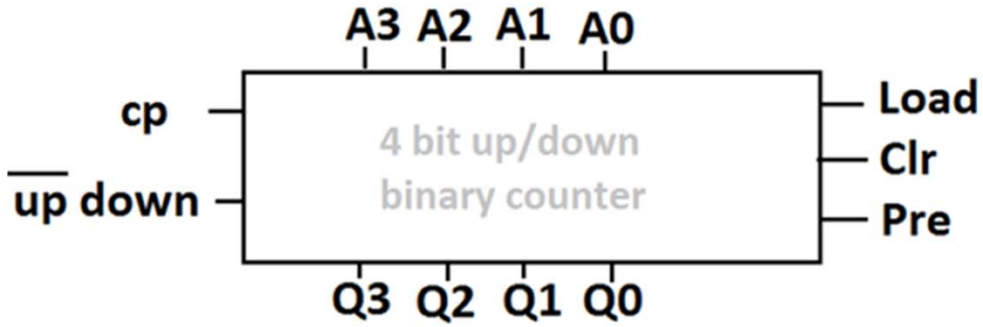


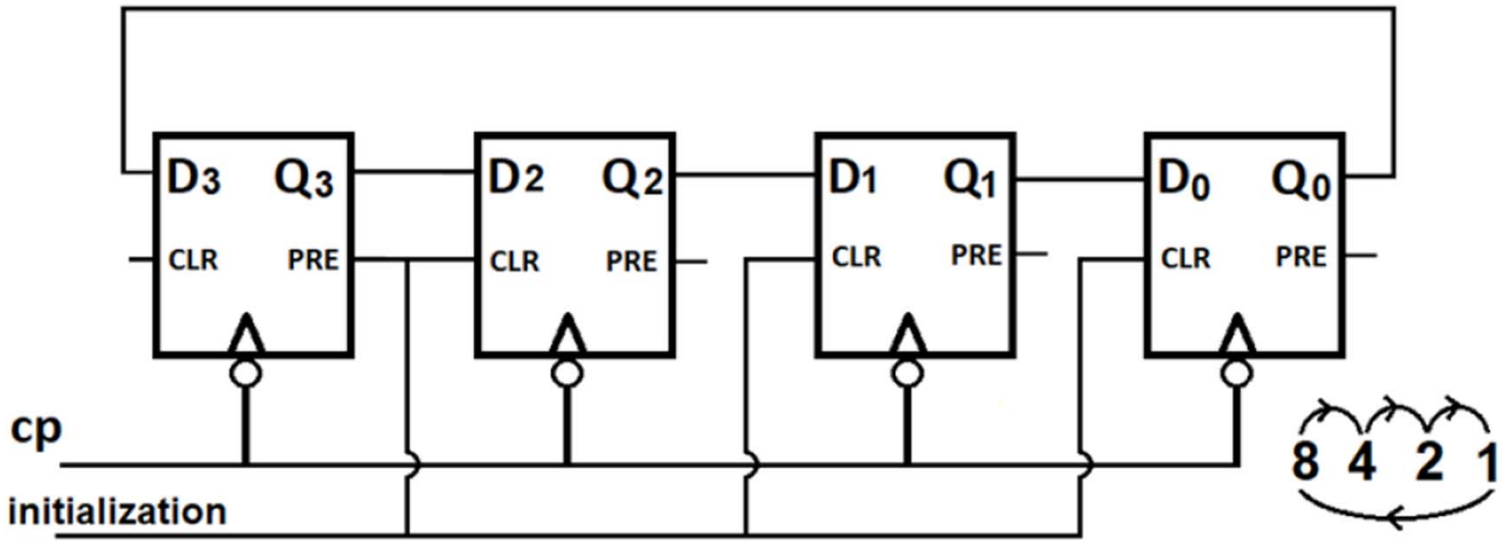
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
:

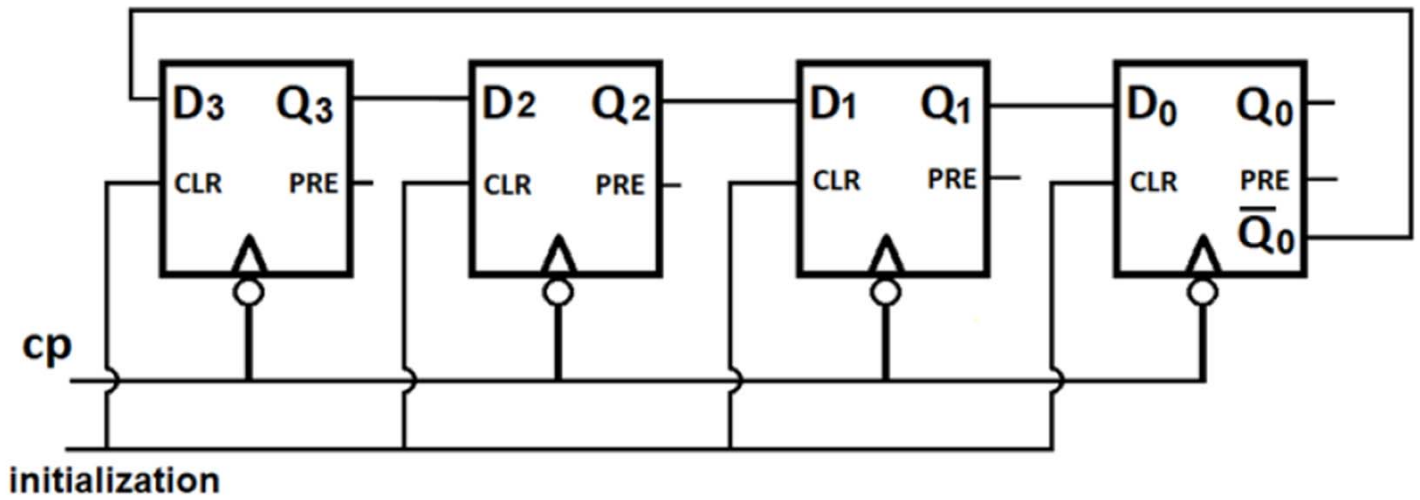


شمارنده نزولی

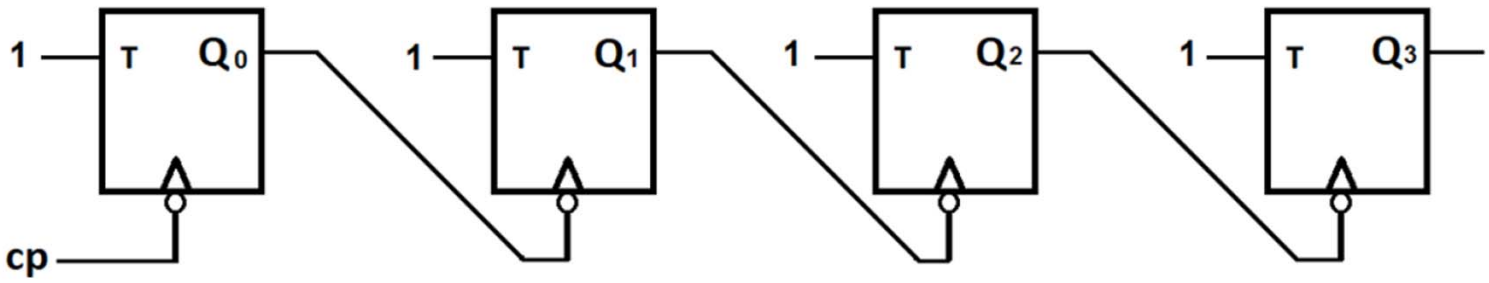

0 up
1 down
1
T0 Q0
T1 Q1
T2 Q2
T3 Q3
Q̄3
cp


A3 A2 A1 A0
cp
up down
4 bit up/down
binary counter
Load
Clr
Pre
Q3 Q2 Q1 Q0

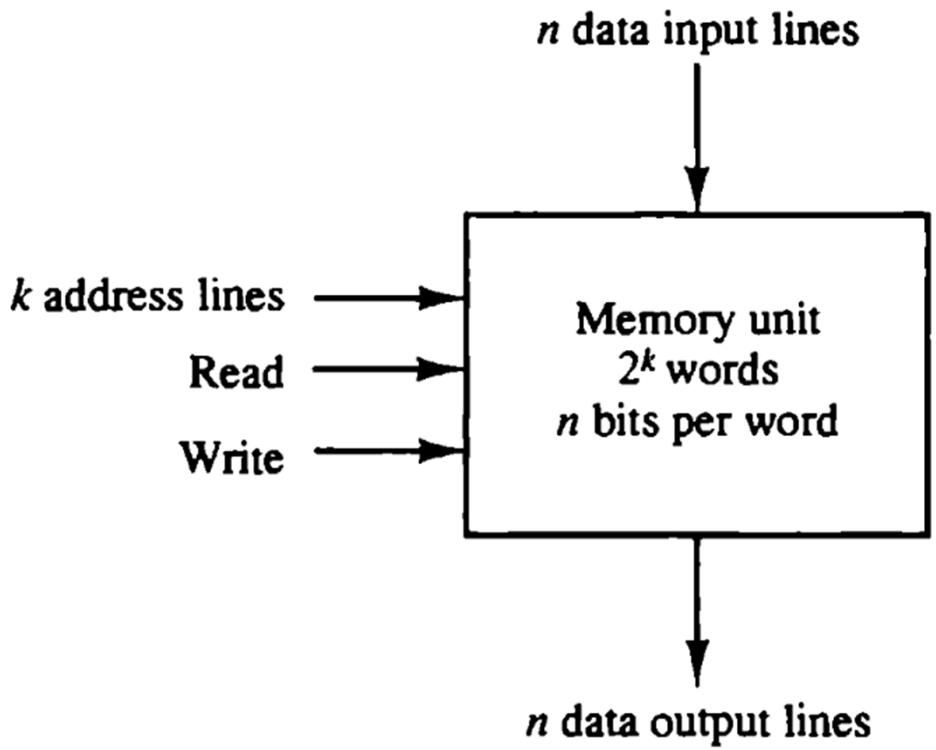

D3
Q3
CLR
PRE
D2
Q2
CLR
PRE
D1
Q1
CLR
PRE
D0
Q0
CLR
PRE
cp
initialization
8 4 2 1



0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1



شمارنده آسنکرون


n data input lines
k address lines
Read
Write
Memory unit
2^k words
n bits per word
n data output lines

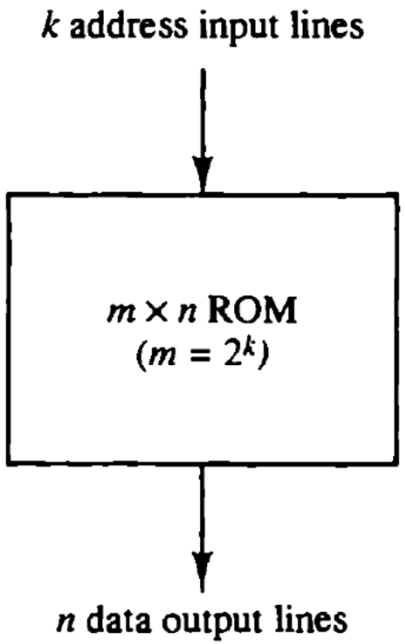


Figure 2-13 Block diagram of read only memory (ROM).

لیست تمرین های مهم فصل دو

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- ۴
- ۷
- ۱۲
- ۱۹
- ۲۲