
معماری کامپیوتر

جلسه چهارم: زبان انتقال بین ثبات ها

فصل چهارم کتاب موریس مانو – طراحی واحد محاسبه و منطق

- زبان انتقال بین ثبات ها
- گذرگاه داده
- بافر سه حالته
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- واحد محاسبه
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زبان انتقال بین ثبات ها

$R2 \leftarrow R1$

If $(P = 1)$ *then* $(R2 \leftarrow R1)$ $\quad P: \quad R2 \leftarrow R1$

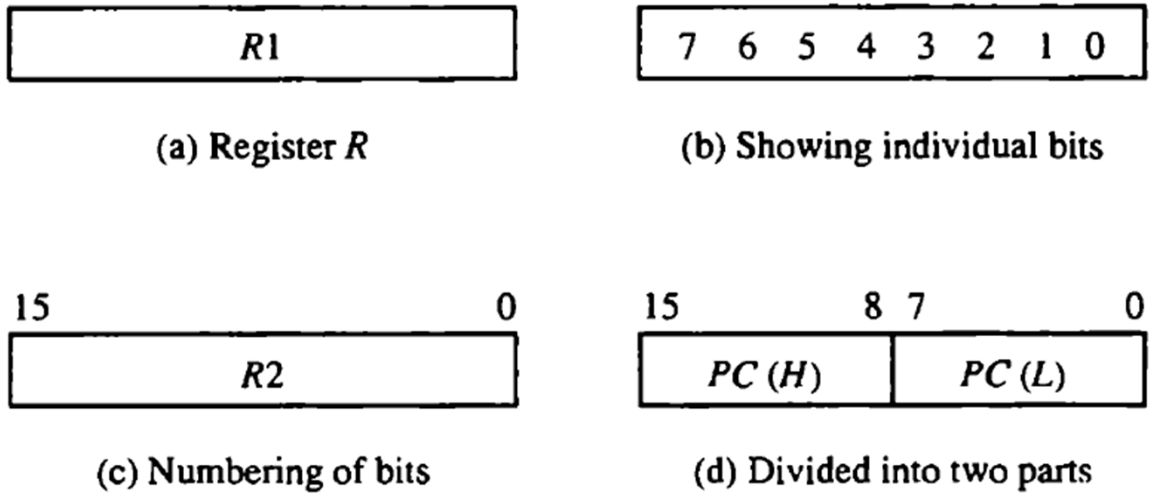
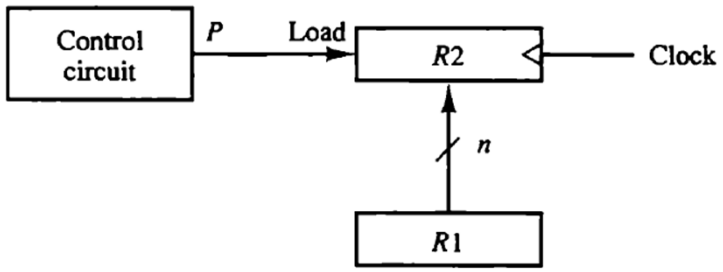


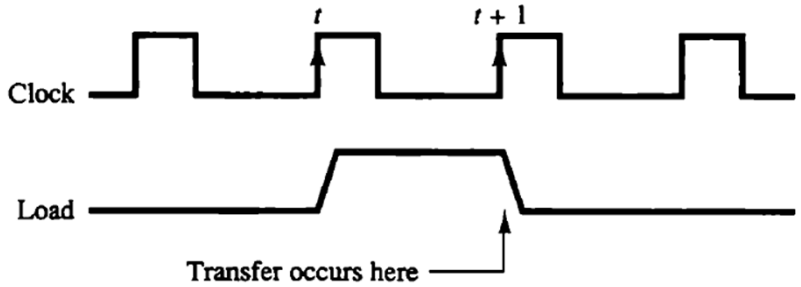
Figure 4-1 Block diagram of register.

زبان انتقال بین ثبات ها با توجه به پالس ساعت

Figure 4-2 Transfer from R1 to R2 when P = 1.



(a) Block diagram



جدول زبان انتقال بین ثبات ها

TABLE 4-1 Basic Symbols for Register Transfers

Symbol	Description	Examples
Letters (and numerals)	Denotes a register	*MAR*, *R2*
Parentheses ( )	Denotes a part of a register	*R2*(0–7), *R2*(*L*)
Arrow ←	Denotes transfer of information	*R2* ← *R1*
Comma ,	Separates two microoperations	*R2* ← *R1*, *R1* ← *R2*

T: $R2 \leftarrow R1, \quad R1 \leftarrow R2$

گذرگاه داده

Figure 4-3 Bus system for four registers.

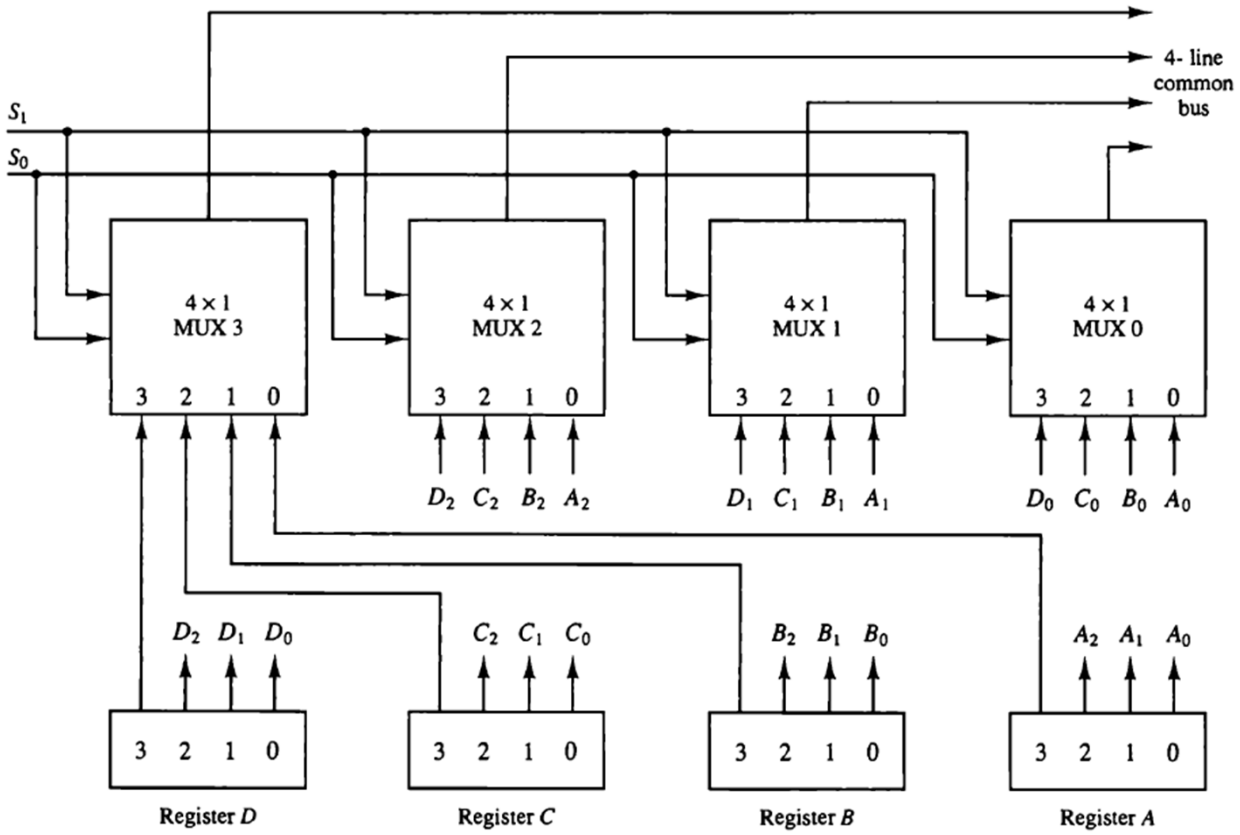


TABLE 4-2 Function Table for Bus of Fig. 4-3

S_1	S_0	Register selected
0	0	A
0	1	B
1	0	C
1	1	D

بافر سه حالته

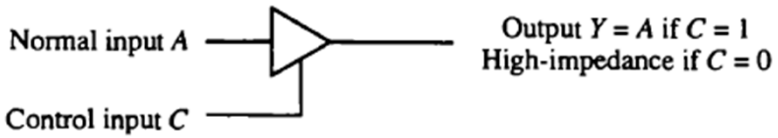


Figure 4-4 Graphic symbols for three-state buffer.

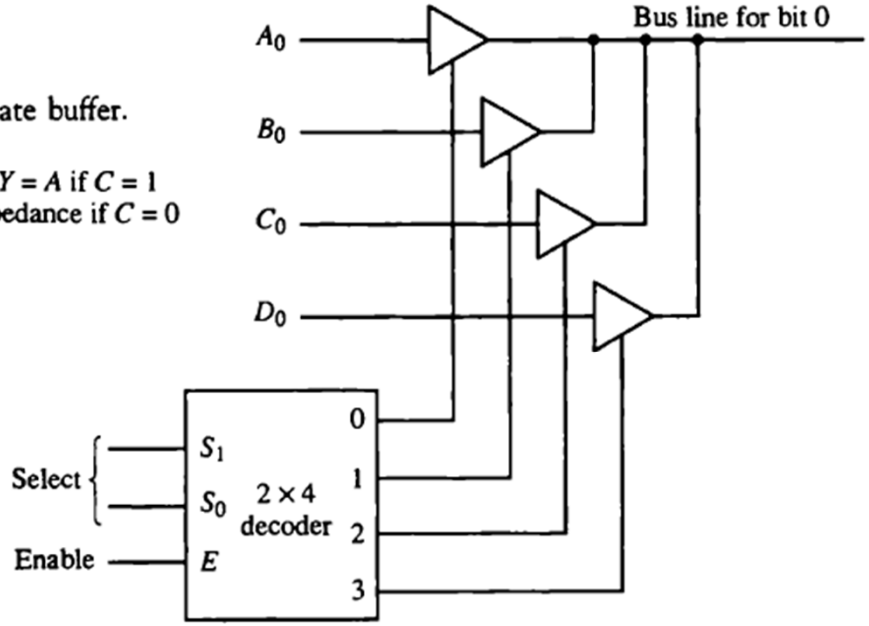


Figure 4-5 Bus line with three state-buffers.

جدول عملگرهای حسابی

TABLE 4-3 Arithmetic Microoperations

Symbolic designation	Description
$R3 \leftarrow R1 + R2$	Contents of $R1$ plus $R2$ transferred to $R3$
$R3 \leftarrow R1 - R2$	Contents of $R1$ minus $R2$ transferred to $R3$
$R2 \leftarrow \overline{R2}$	Complement the contents of $R2$ (1's complement)
$R2 \leftarrow \overline{R2} + 1$	2's complement the contents of $R2$ (negate)
$R3 \leftarrow R1 + \overline{R2} + 1$	$R1$ plus the 2's complement of $R2$ (subtraction)
$R1 \leftarrow R1 + 1$	Increment the contents of $R1$ by one
$R1 \leftarrow R1 - 1$	Decrement the contents of $R1$ by one

جمع و تفریق کننده

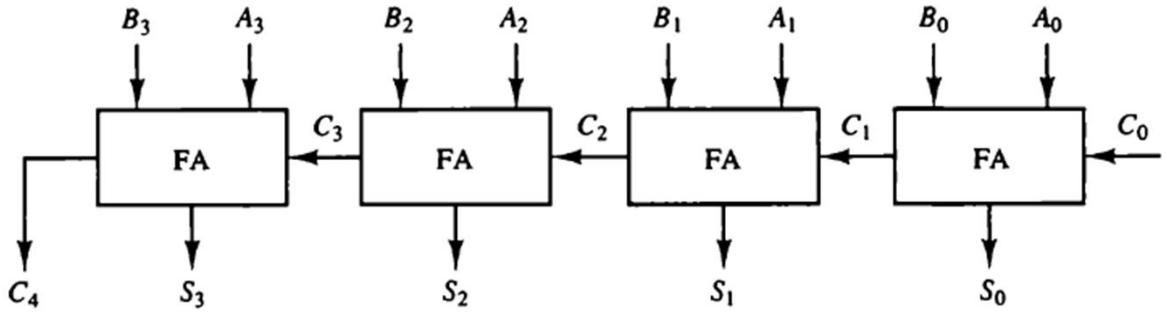


Figure 4-6 4-bit binary adder.

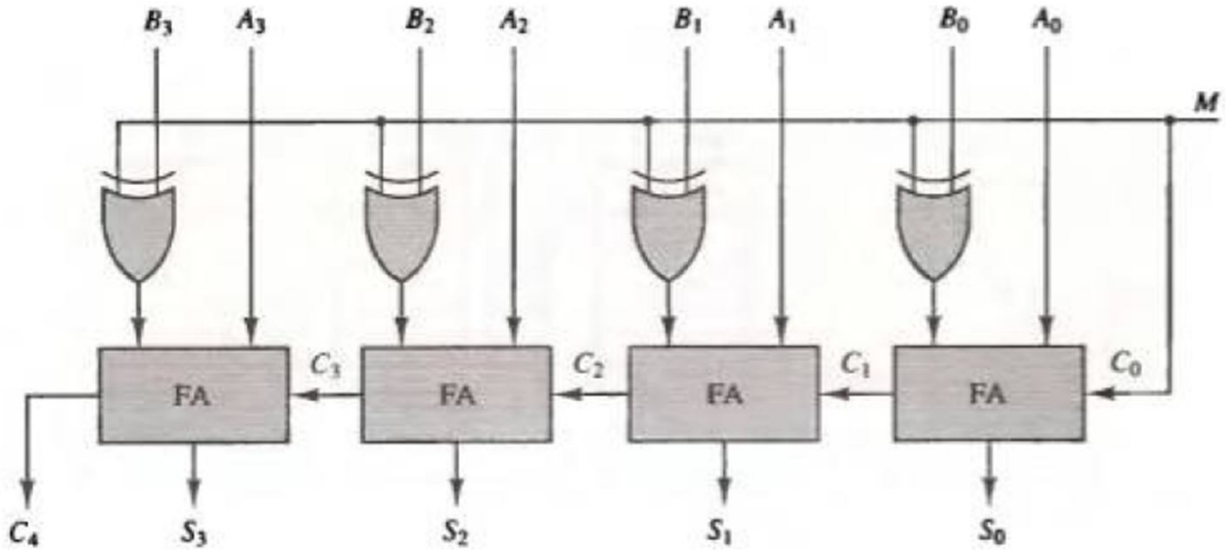
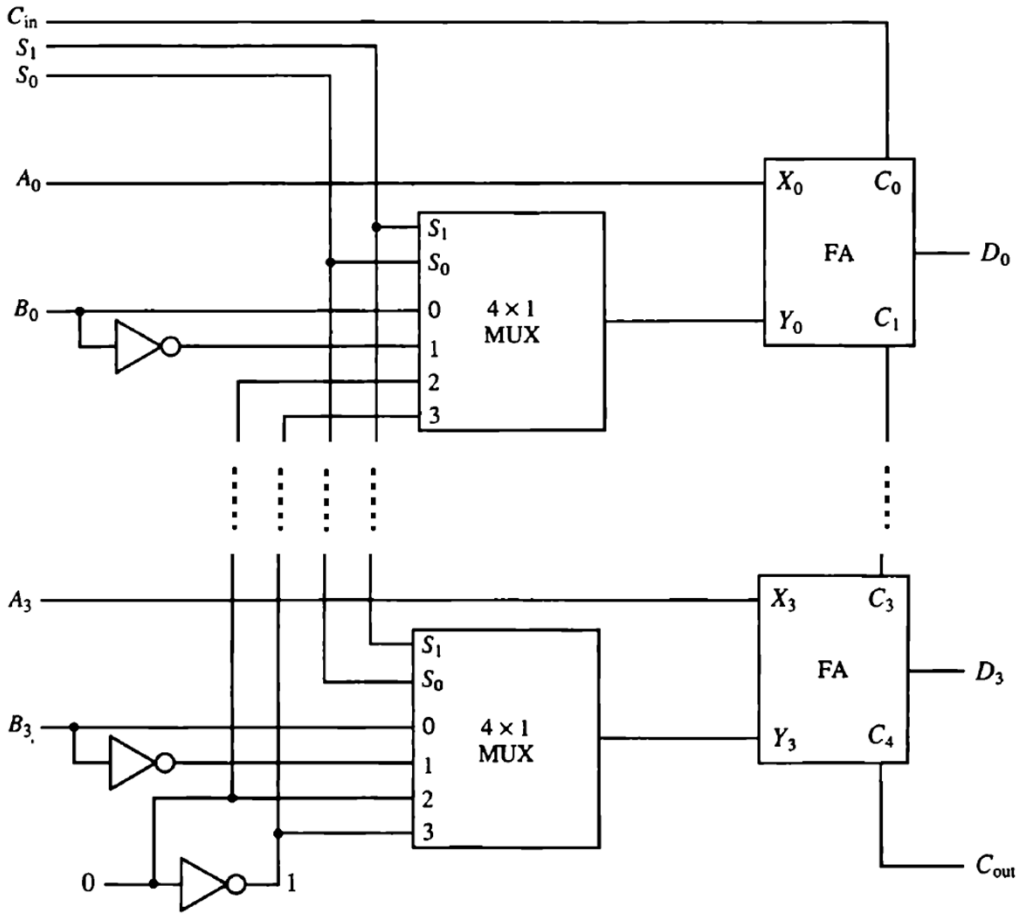
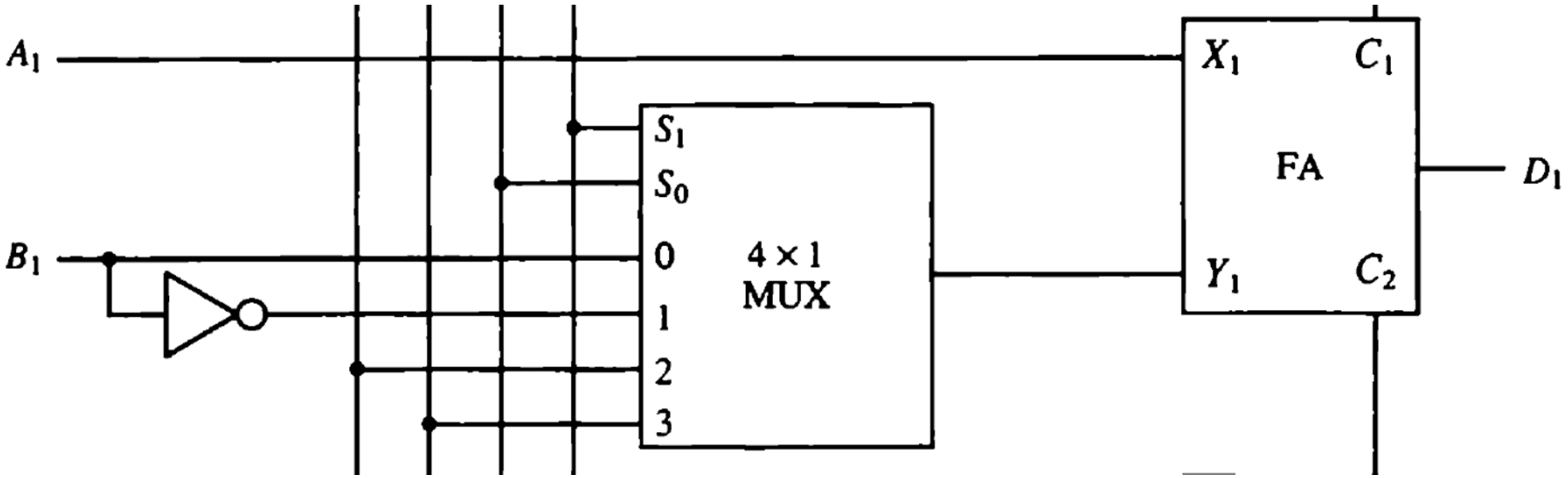


Figure 4-7 4-bit adder-subtractor.

واحد محاسبه


C_{in}
S_1
S_0
A_0
B_0
S_1
S_0
0
1
2
3
4 × 1
MUX
X_0
C_0
FA
Y_0
C_1
D_0
A_3
B_3
S_1
S_0
0
1
2
3
4 × 1
MUX
X_3
C_3
FA
Y_3
C_4
D_3
C_{out}
0
1

واحد محاسبه



واحد محاسبه

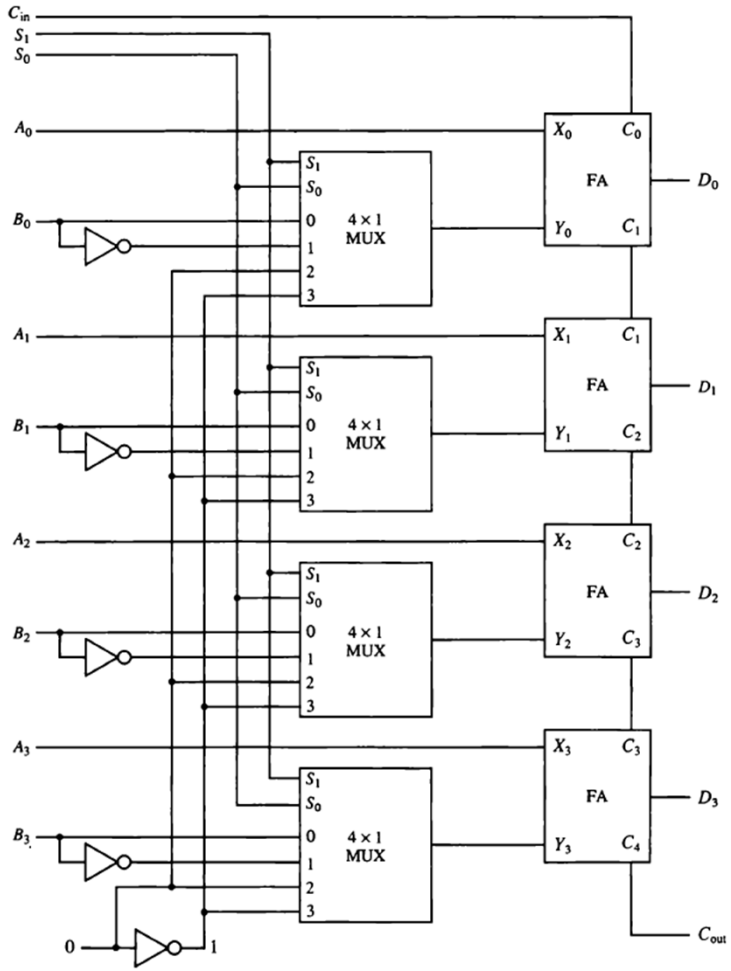


Figure 4-9 4-bit arithmetic circuit.

جدول توابع محاسبه

TABLE 4-4 Arithmetic Circuit Function Table

Select			Input	Output	
S_1	S_0	C_{in}	Y	$D = A + Y + C_{in}$	Microoperation
0	0	0	B	$D = A + B$	Add
0	0	1	B	$D = A + B + 1$	Add with carry
0	1	0	$\overline{B}$	$D = A + \overline{B}$	Subtract with borrow
0	1	1	$\overline{B}$	$D = A + \overline{B} + 1$	Subtract
1	0	0	0	$D = A$	Transfer A
1	0	1	0	$D = A + 1$	Increment A
1	1	0	1	$D = A - 1$	Decrement A
1	1	1	1	$D = A$	Transfer A

جدول توابع منطقی

P: $R1 \leftarrow R1 \oplus R2$

1010	Content of $R1$
1100	Content of $R2$
0110	Content of $R1$ after $P = 1$

$P + Q$: $R1 \leftarrow R2 + R3, \quad R4 \leftarrow R5 \vee R6$

TABLE 4-5 Truth Tables for 16 Functions of Two Variables

x	y	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}	F_{11}	F_{12}	F_{13}	F_{14}	F_{15}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

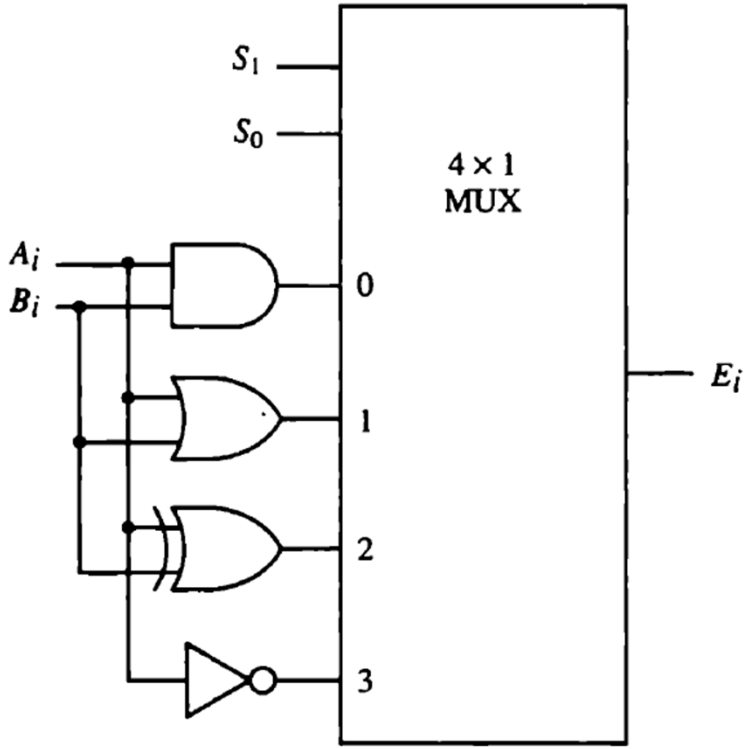
جدول توابع منطقی

TABLE 4-6 Sixteen Logic Microoperations

Boolean function	Microoperation	Name
$F_0 = 0$	$F \leftarrow 0$	Clear
$F_1 = xy$	$F \leftarrow A \wedge B$	AND
$F_2 = xy'$	$F \leftarrow A \wedge \overline{B}$	
$F_3 = x$	$F \leftarrow A$	Transfer A
$F_4 = x'y$	$F \leftarrow \overline{A} \wedge B$	
$F_5 = y$	$F \leftarrow B$	Transfer B
$F_6 = x \oplus y$	$F \leftarrow A \oplus B$	Exclusive-OR
$F_7 = x + y$	$F \leftarrow A \vee B$	OR
$F_8 = (x + y)'$	$F \leftarrow \overline{A \vee B}$	NOR
$F_9 = (x \oplus y)'$	$F \leftarrow \overline{A \oplus B}$	Exclusive-NOR
$F_{10} = y'$	$F \leftarrow \overline{B}$	Complement B
$F_{11} = x + y'$	$F \leftarrow A \vee \overline{B}$	
$F_{12} = x'$	$F \leftarrow \overline{A}$	Complement A
$F_{13} = x' + y$	$F \leftarrow \overline{A} \vee B$	
$F_{14} = (xy)'$	$F \leftarrow \overline{A \wedge B}$	NAND
$F_{15} = 1$	$F \leftarrow$ all 1's	Set to all 1's

یک واحد مدار منطقی

Figure 4-10 One stage of logic circuit.

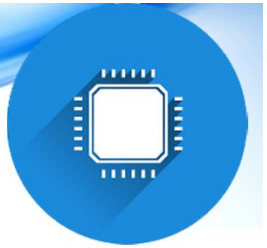


(a) Logic diagram

S_1	S_0	Output	Operation
0	0	$E = A \wedge B$	AND
0	1	$E = A \vee B$	OR
1	0	$E = A \oplus B$	XOR
1	1	$E = \overline{A}$	Complement

(b) Function table

selective-set	1010	*A* before
	1100	*B* (logic operand)
	1110	*A* after
selective-complement	1010	*A* before
	1100	*B* (logic operand)
	0110	*A* after
selective-clear	1010	*A* before
	1100	*B* (logic operand)
	0010	*A* after



0110 1010	*A* before
0000 1111	*B* (mask)
0000 1010	*A* after masking

0000 1010	*A* before
1001 0000	*B* (insert)
1001 1010	*A* after insertion

1010	*A*
1010	*B*
0000	$A \leftarrow A \oplus B$

$R1 \leftarrow \text{shl } R1$

$R2 \leftarrow \text{shr } R2$

TABLE 4-7 Shift Microoperations

Symbolic designation	Description
$R \leftarrow \text{shl } R$	Shift-left register R
$R \leftarrow \text{shr } R$	Shift-right register R
$R \leftarrow \text{cil } R$	Circular shift-left register R
$R \leftarrow \text{cir } R$	Circular shift-right register R
$R \leftarrow \text{ashl } R$	Arithmetic shift-left R
$R \leftarrow \text{ashr } R$	Arithmetic shift-right R

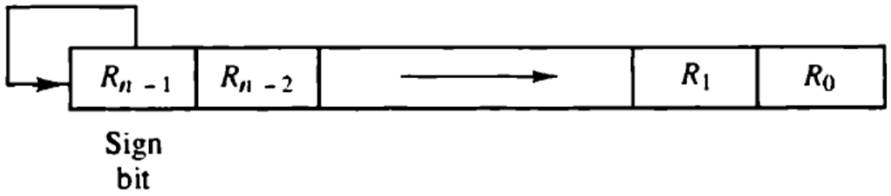
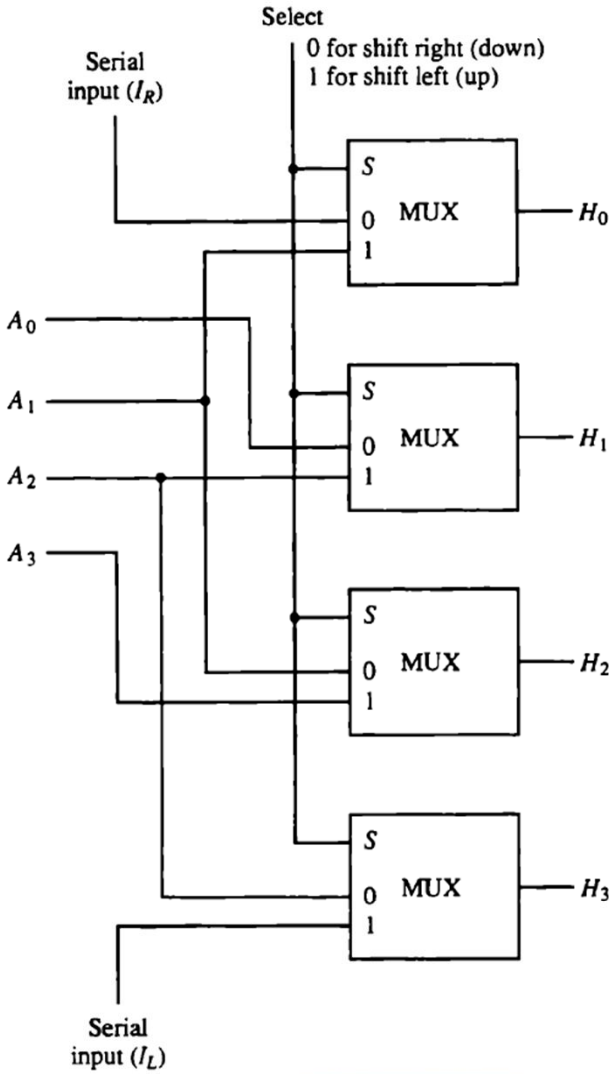


Figure 4-11 Arithmetic shift right.



Function table

Select	Output			
S	H_0	H_1	H_2	H_3
0	I_R	A_0	A_1	A_2
1	A_1	A_2	A_3	I_L

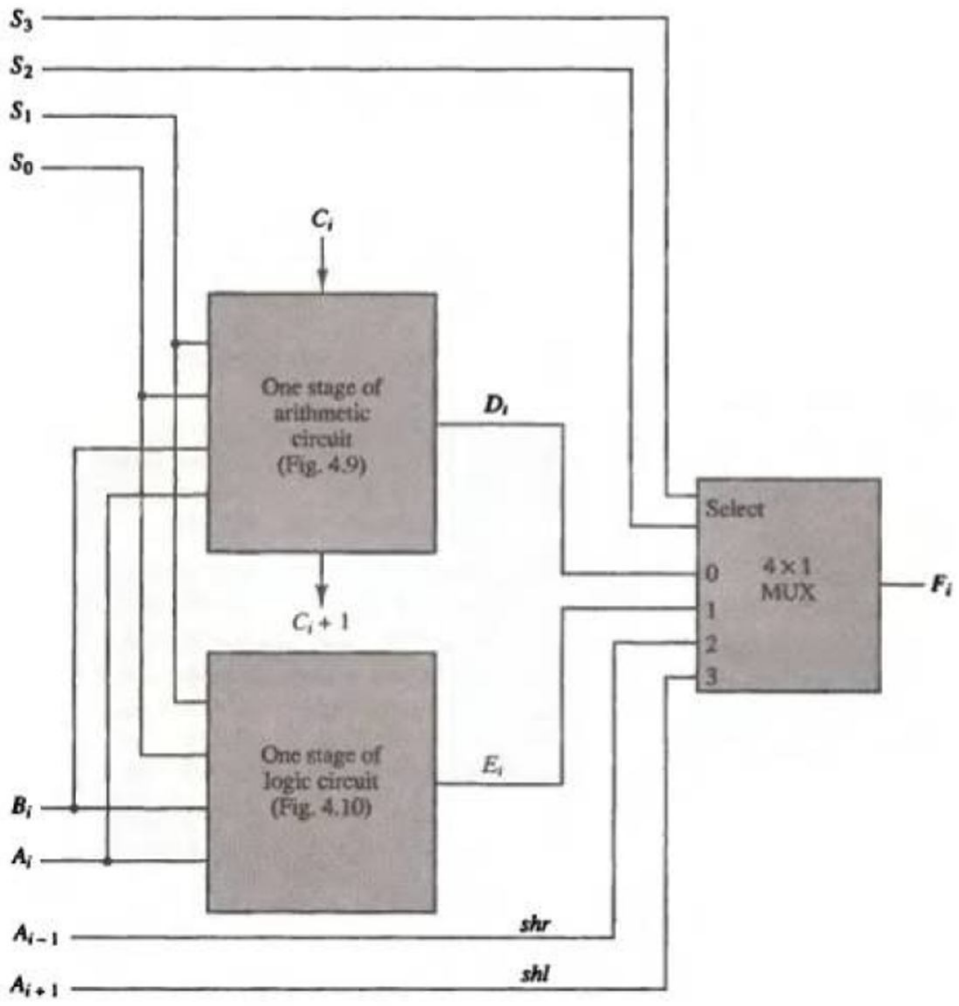

S_3
S_2
S_1
S_0
C_i
One stage of arithmetic circuit (Fig. 4.9)
D_i
$C_i + 1$
Select
0
1
2
3
4 × 1 MUX
F_i
One stage of logic circuit (Fig. 4.10)
E_i
B_i
A_i
A_{i-1}
shr
A_{i+1}
shl

TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

Operation select						
S_3	S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	0	$F = A$	Transfer A
0	0	0	0	1	$F = A + 1$	Increment A
0	0	0	1	0	$F = A + B$	Addition
0	0	0	1	1	$F = A + B + 1$	Add with carry
0	0	1	0	0	$F = A + \overline{B}$	Subtract with borrow
0	0	1	0	1	$F = A + \overline{B} + 1$	Subtraction
0	0	1	1	0	$F = A - 1$	Decrement A
0	0	1	1	1	$F = A$	Transfer A
0	1	0	0	×	$F = A \wedge B$	AND
0	1	0	1	×	$F = A \vee B$	OR
0	1	1	0	×	$F = A \oplus B$	XOR
0	1	1	1	×	$F = \overline{A}$	Complement A
1	0	×	×	×	$F = \text{shr } A$	Shift right A into F
1	1	×	×	×	$F = \text{shl } A$	Shift left A into F

لیست تمرین های مهم فصل چهار

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